rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Claims 1, 2, 4-8 and 10-12 are rejected under 35 U.S.C. §102(e) as being anticipated by Chan et al., U.S. Patent No. 6,051,467.

Claims 3, 9, 14 and 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Chan et al. in view of Applicants' admitted prior art.

Claims 1-12, 14 and 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Yamauchi et al., US Patent No. 5,962,889, or Wu, U.S. Patent No. 6,033,956, or Yamagishi et al., U.S. Patent No. 5,808,339, taken with Ogura et al., U.S. Patent No. 5,672,892, or Hong, U.S. Patent No. 5,478,767, in view of Applicants' admitted prior art.

It is respectfully requested that the objections and rejections set forth in the Office Action be reconsidered and withdrawn in light of the amendments and arguments provided below.

Rejection of Claims Under 35 U.S.C. §112, §132

Claims 1 and 7 are rejected by the Examiner under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. The Examiner has also objected to the language: "forming an oxide on exposed surfaces of the floating gate," as new matter under 35 U.S.C. §132. Applicants have amended claims 1 and 7 to delete this language. Accordingly, claims 1 and 7 as amended should be in condition for allowance.

Claims 1-12, 14 and 15 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. The Examiner directed his rejection specifically against the phrase, "forming an oxide on exposed surfaces of the floating gate," in Claim 1, and the

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

term, "the insulator," in Claim 8. As discussed above, Applicants have deleted the phrase, "forming an oxide on exposed surfaces of the floating gate," in Claim 1, and have canceled Claim 8. Accordingly, Claim 1, as amended, is no longer indefinite, and should be in condition for allowance.

Rejection of Claims Under 35 U.S.C. §102

Claims 1, 2, 4-8 and 10-12 are rejected under 35 U.S.C. §102(e) as being anticipated by Chan et al., U.S. Patent No. 6,051,467. Applicants have amended Claim 1 to claim "depositing an insulator layer of high temperature oxide ... operable to prevent charge leaking from the floating gate," and "depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer." Applicants' original claims and the Specification, page 4, lines 25-27 and FIG. 7 support the added language. The term "high temperature oxide" is well understood by those skilled in the art.[1]

Chan et al. do not teach an insulator layer of high temperature oxide. To the contrary, Chan et al. teach forming "[s]idewall spacers 24 of silicon oxide or silicon nitride ... on the sidewalls of the floating gate," and depositing "an oxide layer ... over the substrate by atmospheric pressure chemical vapor deposition (APCVD) or plasma-enhanced chemical vapor deposition (PECVD)." (Column 3, lines 6-13). There is no indication that the oxide layers disclosed in Chan et al. are "high temperature" oxides. Also, Chan et al. teach two steps to form an oxide layer and an insulator layer, while the method in accordance with Claim 1 involves only one step to form a high temperature oxide serving to both insulate and prevent charges from leaking. Applicants' method has a further advantage in that the high temperature oxide has well-known properties, such as excellent uniformity and small grain size,[2] that improve the planarity of the deposited surface.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

[1] S. Wolf and R.N. Tauber, Silicon Processing for the VLSI Era, Vol. 1 - Process Technology p. 184 (Lattice Press, 1986) (high temperature oxides are often formed by an LPCVD process); Buried-Channel PMOSFET Elevated Source/Drain Using Self-Aligned Epitaxial Silicon Silver, Abstract, Senior Semiconductor Society, currently accessible at http://www.semicontech.com/korean/se2/se2-1a02.html.

[2] S. Wolf, p. 169.

Chan et al. also do not teach "depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer." Chan et al. disclose depositing "a thin layer of polysilicon 32 ... over the polished surface of the substrate," then "the ONO interpoly dielectric 36 is deposited." (Column 3, lines 28-47). Chan et al. teach that polysilicon layer 32 is a "key" feature that provides a desirable grain size, avoids implantation damage (Column 3, lines 38-45), and provides an avenue for varying the width of control gate (Column 4, lines 6-9). Chan et al. teach away from Claim 1 because to modify Chan et al. in the direction of Applicants' claim would destroy the utility of Chan et al.'s disclosed device. Accordingly, Claim 1 as amended distinguishes over the cited prior art and should be in condition for allowance.

Claim 7 has been similarly amended, and claims "depositing an insulator layer of high temperature oxide," and "depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer." Therefore, for reasons similar to those given above with respect to Claim 1, Claim 7 as amended distinguishes over the cited prior art and should be in condition for allowance.

Claims 2 and 8 have been canceled. Claims 3-6 and 9-12, 14, 15 are dependent upon Claim 1 and Claim 7, respectively, and should therefore be allowed by virtue of being dependent upon allowable claims.

Rejection of Claims Under 35 U.S.C. §103

Applicants' claims 3, 9, 14 and 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Chan et al. in view of Applicants' admitted prior art. These claims are dependent upon Claim 1 or Claim 7 and should therefore be allowable for at least the same reasons discussed above with respect to Claim 1 and Claim 7.

Claims 1-12 and 14-15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Yamauchi et al., Wu or Yamagishi et al. taken with Ogura et al. or Hong in view of

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

Applicants' admitted prior art. It is respectfully submitted that the cited references do not teach or disclose Applicants' method as recited in claims 1 and 7.

Yamauchi et al. teach deposition of a polysilicon layer 15 prior to the deposition of the dielectric layer, ONO film 9. Further, Yamauchi et al. only teach the chemical vapor deposition of a silicon oxide. In contrast to these teachings, Applicants, in Claim 1, recite "depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer," as well as "depositing an insulator layer of high temperature oxide." By depositing the dielectric layer directly over the exposed top surface of the floating gate and the insulator layer, the lithographical patterning and etching of the polysilicon control gate is facilitated in a subsequent step. Applicants' use of the high temperature oxide also provides advantages over Yamauchi et al., preventing charge leaking from the floating gate, and providing a more planar surface for the subsequent layers.

Claim 7 is similarly amended, and claims "depositing an insulator layer of high temperature oxide," and "depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer." Therefore, for reasons given above with respect to Claim 1, Claim 7 as amended distinguishes over Yamauchi et al.

For the insulator layer, Wu teaches the chemical vapor deposition of a conformal tetraethyl orthosilicate oxide, 210. Further, Wu teaches the use of a planarizing plasma etch (Column 1, lines 52-58) and a liquid-phase depositing technique (Column 3, lines 10-14) to provide the insulator layer. In contrast to these teachings, Applicants' claims 1 and 7, recite "depositing an insulator layer of high temperature oxide," and then "polishing the insulator layer." By using a high temperature oxide, present method allows one to polish the insulator layer using conventional chemical-mechanical techniques. This thereby provides a planar surface less expensively, and prevents charge leaking from the floating gate by using such an oxide.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

Yamagishi et al. teach the deposition of a planarizing insulating layer 116, but do not disclose the composition or functionality of this layer. In contrast, Applicants, in claims 1 and 7 recite "depositing an insulator layer of high temperature oxide." This oxide has improved planarity and prevents charge leaking from the floating gate. Therefore, claims 1 and 7 distinguish over Yamagishi.

Ogura et al. and Hong teach thermal oxidation, but do not teach the deposition of a high temperature oxide. Neither Ogura et al., nor Hong, nor Applicants' prior art remedy the deficiencies of Yamauchi et al, Wu, or Yamagishi et al. as discussed above with respect to claims 1 and 7. Accordingly, claims 1 and 7 as amended distinguish over the cited prior art and should be in condition for allowance.

Claims 3-6 are dependent upon Claim 1 and should therefore be allowed by virtue of being dependent upon an allowable claim. Similarly, claims 9-12, 14 and 15 are dependent upon Claim 7 and should therefore be allowed by virtue of being dependent upon an allowable claim.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned.

EXPRESS MAIL LABEL NO:

EL849436115US

Respectfully submitted,

F. Jason Far-hadian
Attorney for Applicant(s)
Reg. No. 42,523

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

ATTACHMENT A

1. (Twice Amended) A method of making a flash memory cell including a substrate and a floating gate, the method comprising:

[forming an oxide on exposed surfaces of the floating gate;]

depositing an insulator layer of high temperature oxide on the substrate and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and operable to prevent charge leaking from the floating gate;

polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

2. Canceled.

7. (Twice Amended) A method of making a flash memory cell having a substrate and a tunnel oxide formed on the substrate, the method comprising:

depositing a floating gate layer on the tunnel oxide to a first thickness;

etching the floating gate layer, to provide a floating gate;

[forming an oxide on exposed surfaces of the floating gate;]

depositing an insulator layer of high temperature oxide on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness;

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

8. Canceled.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979